CLAIMS

1. A processor comprising:

a heat release frequency holding unit which holds a heat release frequency of a plurality of blocks subject to heat release control;

a heat release identifying unit which identifies a block involved in the execution of each execution unit comprising at least one instruction, and which identifies a heat release coefficient related to a heat value of the identified block; and

a heat release frequency adder unit which cumulatively increases, for each execution unit, the heat release frequency of the identified block by referring to the heat release coefficient, as the execution of instructions proceeds.

2. The processor according to claim 1, wherein the heat release identifying unit is a decoder for decoding instructions to be executed.

3. The processor according to claim 1, further comprising a heat release frequency subtractor unit which subtracts from the heat release frequency of the blocks in accordance with heat discharge that occurs with time.

4. The processor according to claim 3, wherein the heat release frequency subtractor unit subtracts such that the larger the heat release frequency of the operational block, the larger the amount of subtraction.

5. A processor comprising:

a heat release frequency holding unit which holds a heat release frequency of a plurality of blocks subject to heat release control;

a heat release frequency adder unit which cumulatively increases, for each execution unit comprising at least one instruction, the heat release frequency of a block involved in the execution of the execution unit by referring to a heat value estimated for the execution unit, as the execution of instructions proceeds; and

a scheduler which schedules instructions to be executed in accordance with the heat release frequency of the blocks.

6. The processor according to claim 5, wherein the scheduler delays the execution of instructions involving a block with its heat release frequency exceeding a predetermined threshold value.

7. The processor according to claim 5, further comprising a heat release frequency subtractor unit which subtracts from the heat release frequency of the blocks in accordance with

heat discharge that occurs with time.

8. A processor comprising:

a heat release frequency holding register which holds a heat release frequency of a plurality of blocks subject to heat release control;

a heat release coefficient profile which stores, in correspondence with each other, an instruction to be executed, a block involved in the execution of the instruction and a heat release coefficient related to a heat value of the involved block;

a decoder which analyzes an instruction to be executed so as to identify, for each execution unit comprising at least one instruction, the block involved in the execution of the instruction and the associated heat release coefficient, and which stores identified information in the heat release coefficient profile;

a heat release frequency adder unit which cumulatively increases, for each execution unit, the heat release frequency of the identified block by referring to the heat release coefficient profile, as the execution of instructions proceeds; and

a scheduler which schedules instructions to be executed in accordance with the heat release frequency of the blocks.

9. A multiprocessor system including a plurality of

subprocessors and a main processor, wherein the main processor comprises:

a heat release frequency holding register which holds a heat release frequency of a plurality of blocks in each of the subprocessors;

a heat release identifying unit which identifies a block involved in the execution of each execution unit comprising at least one instruction, and which identifies a heat release coefficient related to a heat value of the identified block;

a heat release frequency adder unit which cumulatively increases, for each execution unit, the heat release frequency of the identified block by referring to the heat release coefficient, as the execution of instructions proceeds; and

a scheduler which allocates instructions to be executed among the plurality of subprocessors in accordance with the heat release frequency of the blocks.

10. A processor in which a decoder for decoding an instruction to be executed is provided with the function of analyzing heat release of a block in the processor involved in the execution of the instruction.

11. A temperature control method in which heat release occurring as instruction codes are executed is detected in

units of blocks, by cumulatively increasing, for each execution unit comprising at least one instruction, a heat release frequency of a block involved in the execution of the execution unit, as the execution of instruction codes proceeds, and by holding the accumulated heat release frequency in a register.

12. A temperature control method which cumulatively increases, for each execution unit comprising at least one instruction, a heat release frequency of a block involved in the execution of the execution unit by referring to a heat value estimated for the execution unit, as the execution of instructions proceeds, which holds the accumulated heat release frequency in a register, and which schedules instructions to be executed in accordance with the heat release frequency of blocks held in the register.

13. A temperature control method which estimates, for each execution unit comprising at least one instruction, a heat value of blocks in each of processors in a multiprocessor system, which predicts temperature variation in the blocks as the execution of instructions proceeds, and which allocates instructions to the processors in accordance with the predicted temperature variation.

14. A program which causes a computer to execute the steps

of:

cumulatively increasing, for each execution unit comprising at least one instruction, a heat release frequency of a block involved in the execution of the execution unit, as the execution of instruction codes proceeds, and holding the accumulated heat release frequency in a register; and

detecting heat release occurring as the instruction codes are executed in units of blocks, in accordance with the heat release frequency of the blocks held in the register.

15. A program which causes a computer to execute the steps of:

cumulatively increasing, for each execution unit comprising at least one instruction, a heat release frequency of a block involved in the execution of the execution unit by referring to a heat value estimated for the execution unit, as the execution of instructions proceeds; and

scheduling instructions to be executed in accordance with the heat release frequency of blocks held in the register.

16. A program which causes a computer to execute the steps of:

estimating, for each execution unit comprising at least one instruction, a heat value of blocks in each of processors in a multiprocessor system; and

predicting temperature variation in the blocks as the execution of instructions proceeds and allocating instructions to the processors in accordance with the predicted temperature variation.

17. A recording medium which stores a program that causes a computer to execute the steps of:

cumulatively increasing, for each execution unit comprising at least one instruction, a heat release frequency of a block involved in the execution of the execution unit, as the execution of instruction codes proceeds, and holding the accumulated heat release frequency in a register; and

detecting heat release occurring as the instruction codes are executed in units of blocks, in accordance with the heat release frequency of the blocks held in the register.

18. A recording medium which stores a program that causes a computer to execute the steps of:

cumulatively increasing, for each execution unit comprising at least one instruction, a heat release frequency of a block involved in the execution of the execution unit by referring to a heat value estimated for the execution unit, as the execution of instructions proceeds; and

scheduling instructions to be executed in accordance with the heat release frequency of blocks held in the register.

19. A recording medium which stores a program that causes a computer to execute the steps of:

estimating, for each execution unit comprising at least one instruction, a heat value of blocks in each of processors in a multiprocessor system; and

predicting temperature variation in the blocks as the execution of instructions proceeds and allocating instructions to the processors in accordance with the predicted temperature variation.

20. A processor system comprising:

a heat release frequency holding unit which holds a heat release frequency of a plurality of blocks subject to heat release control;

a heat release identifying unit which identifies a block involved in the execution of each execution unit comprising at least one instruction, and which identifies a heat release coefficient related to a heat value of the identified block; and

a heat release frequency adder unit which cumulatively increases, for each execution unit, the heat release frequency of the identified block by referring to the heat release coefficient, as the execution of instructions proceeds.

21. A processor system comprising:

a heat release frequency holding unit which holds a heat release frequency of a plurality of blocks subject to heat release control;

a heat release frequency adder unit which cumulatively increases, for each execution unit comprising at least one instruction, the heat release frequency of a block involved in the execution of the execution unit by referring to a heat value estimated for the execution unit, as the execution of instructions proceeds; and

a scheduler which schedules instructions to be executed in accordance with the heat release frequency of the blocks.

22. A processor system comprising:

a heat release frequency holding register which holds a heat release frequency of a plurality of blocks subject to heat release control;

a heat release coefficient profile which stores, in correspondence with each other, an instruction to be executed, a block involved in the execution of the instruction and a heat release coefficient related to a heat value of the involved block;

a decoder which analyzes an instruction to be executed so as to identify, for each execution unit comprising at least one instruction, the block involved in the execution of the instruction and the associated heat release coefficient,

and which stores identified information in the heat release coefficient profile;

a heat release frequency adder unit which cumulatively increases, for each execution unit, the heat release frequency of the identified block by referring to the heat release coefficient profile, as the execution of instructions proceeds; and

a scheduler which schedules instructions to be executed in accordance with the heat release frequency of the blocks.

23. A processor system in which a decoder for decoding an instruction to be executed is provided with the function of analyzing heat release of a block in the processor involved in the execution of the instruction.

24. An information processing apparatus comprising:

a heat release frequency holding unit which holds a heat release frequency of a plurality of blocks subject to heat release control;

a heat release identifying unit which identifies a block involved in the execution of each execution unit comprising at least one instruction, and which identifies a heat release coefficient related to a heat value of the identified block; and

a heat release frequency adder unit which cumulatively increases, for each execution unit, the heat release

frequency of the identified block by referring to the heat release coefficient, as the execution of instructions proceeds.

25. An information processing apparatus comprising:

a heat release frequency holding unit which holds a heat release frequency of a plurality of blocks subject to heat release control;

a heat release frequency adder unit which cumulatively increases, for each execution unit comprising at least one instruction, the heat release frequency of a block involved in the execution of the execution unit by referring to a heat value estimated for the execution unit, as the execution of instructions proceeds; and

a scheduler which schedules instructions to be executed in accordance with the heat release frequency of the blocks.

26. An information processing apparatus comprising:

a heat release frequency holding register which holds a heat release frequency of a plurality of blocks subject to heat release control;

a heat release coefficient profile which stores, in correspondence with each other, an instruction to be executed, a block involved in the execution of the instruction and a heat release coefficient related to a heat value of the involved block;

a decoder which analyzes an instruction to be executed so as to identify, for each execution unit comprising at least one instruction, the block involved in the execution of the instruction and the associated heat release coefficient, and which stores identified information in the heat release coefficient profile;

a heat release frequency adder unit which cumulatively increases, for each execution unit, the heat release frequency of the identified block by referring to the heat release coefficient profile, as the execution of instructions proceeds; and

a scheduler which schedules instructions to be executed in accordance with the heat release frequency of the blocks.

27. An information processing apparatus in which a decoder for decoding an instruction to be executed is provided with the function of analyzing heat release of a block in the processor involved in the execution of the instruction.